ABSTRACT

The serial peripheral interface and high performance buffering scheme according to the present invention addresses many of the shortcomings of the prior art. In accordance with various aspects of the present invention, an improved high performance buffering scheme is provided with a serial peripheral interface (SPI) to enable microcontroller-based products and other components and devices to achieve a higher serial transmit and receive data rate. In accordance with an exemplary embodiment, a SPI comprises a single buffer having a high data rate, for example, at least the throughput of double buffer schemes, but without the increased size in logic area. To facilitate the throughput of data, the SPI single buffer can be configured with a queuing arrangement. The queuing arrangement for the SPI single buffer can comprise any queuing configuration, such as, for example, a circular queuing arrangement or a linear queuing arrangement. Through operation of the queuing arrangement, the SPI can be configured to provide for the receiving of new data in a register at substantially the same time that stored data can be transmitted to another device, thus the SPI can realize a high data rate. In accordance with an exemplary embodiment, a queuing arrangement is configured in a FIFO buffer having a pointer and counter arrangement. In addition the buffering scheme can provide a high data rate without requiring frequent CPU polling or high interrupt overhead wherein the buffering scheme is configured with an interrupt configuration for identifying when data is ready for transmitting or for reading by the CPU.